



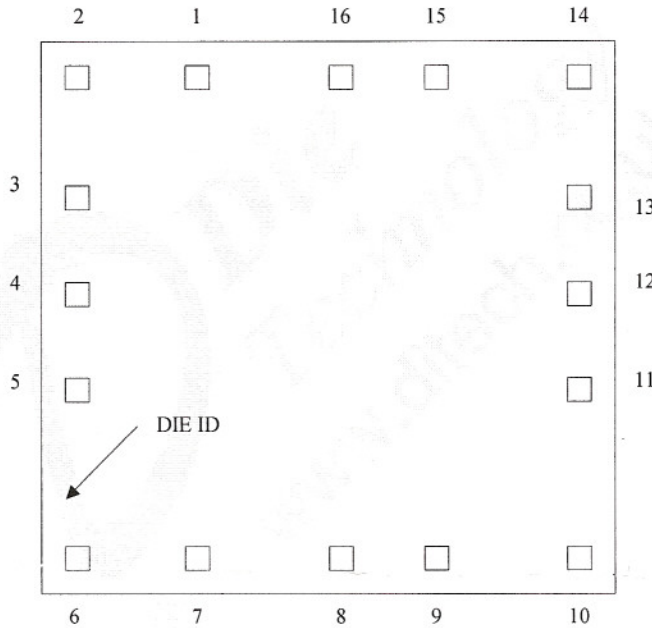
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PAD FUNCTIONS

1	NOTE
2	A
3	B
4	Q0
5	Q1
6	Q2
7	Q3
8	VSS
9	Q3
10	Q2
11	Q1
12	Q0
13	B
14	A
15	NOTE
16	VDD



The information given is believed to be correct at the time of issue.

Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.

Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001inch

<p><u>APPROVED</u></p> <p>BEN WHITE</p> <p>.....</p> <p>DATE: 19/5/2004</p>	<p>CD4555B</p> <p>TI</p>	<p><u>DIE INFORMATION</u></p> <p>DIMENSIONS (Mils): 70 x 67 x 25</p> <p>BOND PADS (Mils):</p> <p>MASK. REF: CD4555B</p> <p>GEOMETRY:</p> <p>BACK POTENTIAL: VCC</p>
<p>DG 10.1.2</p> <p>Rev B, 7/19/02</p>		<p><u>METALLISATION</u></p> <p>TOP: Al</p> <p>BACK: Si</p>